

High mobility 4H-SiC trench gate MOSFETs

Jian Wu, J. Hu, J. H. Zhao, X. Wang, X. Li, T. Burke

A new 4H-SiC trench gate MOSFET structure with epitaxial buried channel improving the channel mobility is reported. Fabricated devices subject to rapid thermal annealing at 850°C for 5 min exhibit a peak field-effect mobility (μ_{FE}) of 104 cm²/Vs at room temperature (25°C) and a high peak μ_{FE} of 269 cm²/Vs at 200°C, which are among the highest levels reported to date.

Introduction: Silicon carbide (SiC) power devices are expected to drastically outperform Si counterparts due to superior physical properties of SiC, such as wide bandgap, high breakdown field and high thermal conductivity. In particular, the 4H-SiC MOSFET is a promising candidate for high power and high temperature applications. However, the development of low on-resistance 4H-SiC MOSFETs has been limited by very low channel mobility, which is attributed to the exponentially increased interface states towards the conduction band, resulting in substantial electron charge trapping and Coulomb scattering at the SiO₂/SiC interface [1]. Recently two approaches have been employed to improve the quality of the MOS interface: First, the nitridation of the MOS interface either by nitric oxide (NO) growth or by NO annealing has achieved peak inversion channel mobility of up to 50 cm²/Vs [2, 3], Second, the use of contamination oxidation in alumina environment rather than the conventional quartz environment during oxidation [4] has been

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reported to improve the inversion channel mobility up to $150 \text{ cm}^2/\text{Vs}$. However, the results in [4] were only achieved under the condition that source and drain contacts did not undergo any rapid thermal annealing for Ohmic contacts, because such treatment may result in a decrease of the field-effect mobility by a factor of about two [5]. Another possible solution for the improvement of the channel mobility is to keep the conduction channel of electrons away from the inferior SiO_2/SiC surface in order for a reduced interfacial trap interaction and inherently higher carrier mobilities. Some researchers reported a buried channel structure formed by ion implantation improved the channel mobility in 4H-SiC MOSFETs up to $140 \text{ cm}^2/\text{Vs}$ [6]. Similar to [5], however, this high mobility was only obtained without contact annealing. It is also noteworthy that ion implantation and subsequent activation anneal at 1500°C , required for buried channels formation, may also damage the quality of SiC surface, resulting in channel mobility degradation. In addition, ion implantation is not a cost-effective process to form buried channels of different depths for the control of the channel mobility and the threshold voltage. In this letter high mobility 4H-SiC trench gate MOSFETs are demonstrated, in which epitaxial layer rather than implanted layer was utilized for the purpose of obtaining superior quality of conduction channel. The depth of the epitaxial buried-channel was conveniently controlled by inductively-coupled plasma (ICP) etching. The devices subject to rapid thermal annealing at 850°C for 5 min exhibited a peak μ_{FE} of $104 \text{ cm}^2/\text{Vs}$ at room temperature and a high peak μ_{FE} of $269 \text{ cm}^2/\text{Vs}$ at 200°C .

Device fabrication: Fig. 1 shows the cross-sectional view of a fabricated 4H-SiC trench-gate MOSFET. The channel length and width of MOSFETs were 15 μm and 350 μm , respectively. Usually a long channel design (100 μm) was adopted in [4-6] for channel mobility evaluation without Ohmic contact annealing, in order to neglect contact resistivity. The starting 4H-SiC 8° off-axis Si face wafer purchased from Cree Inc. had an initial 0.22 μm thick n-type epilayer with a doping concentration of $2 \times 10^{16} \text{ cm}^{-3}$ for buried channels. A 0.79 μm thick p-type epilayer with a doping concentration of $4 \times 10^{17} \text{ cm}^{-3}$ was underneath the channel layer, and a highly doped n-type epilayer (0.15 μm , $N_d = 2 \times 10^{19} \text{ cm}^{-3}$) was grown on the channel layer. The wafer was first etched by ICP in the CF_4/O_2 mixture deep into p layer for mesa isolation. The trench-gate region was then formed by shallow ICP etching, resulting in an adjusted 0.15 μm thick channel region. Thereafter, a sacrificial oxide layer was thermally grown in wet ambient at 1100°C for 0.5 hr and then stripped off by diluted HF acid. A 100nm thick gate oxide layer was grown in a horizontal quartz furnace by a sandwich process [7]: direct oxide growth in nitric oxide (NO) at 1175°C for 18 hr, followed by NO annealing at 950°C for 3 hr; dry O_2 was then used to add thicker oxide at 1175°C for 3 hr; finally the sample was annealed in NO at 1175°C for 3 hr to passivate SiO_2/SiC interface by creating Si \equiv N bonds. The initial nitridation is essential in order to smoothen the interface by removing any accumulated carbon and to passivate the interface. After opening windows in the oxide, 300nm thick Ni was sputtered to form source and drain contacts. 300 nm thick Gate contacts were formed by Mo sputtering. Rapid thermal annealing for Ohmic contacts was performed at 850°C for 5 min in nitrogen forming gas (5% H_2 in N_2).

Characterization: Characterizations were conducted with a HP4145B semiconductor parameter analyzer. Trenched gate MOSFETs with channel current flow perpendicular to the wafer's major flat were tested with source contacts grounded. The output characteristics of a device at room temperature and 200°C are shown in fig. 2a and fig. 2b, respectively. The gate voltage was stepped in 10 V steps safely up to 40 V, corresponding to a strong electric field of 4 MV/cm to the gate oxide. It is seen that the drain currents at 200°C are drastically higher compared to those at room temperature, indicating substantially increased channel mobility at 200°C. Fig. 3a shows the transfer characteristics of a device at room temperature with a small fixed drain voltage of 50 mV. The corresponding field-effect mobility was also calculated and plotted in fig. 3a. It shows the peak μ_{FE} is as high as 104 cm²/Vs, even though the device underwent rapid thermal annealing for Ohmic contacts. It can be inferred that the buried-channel, epitaxially grown for superior quality, effectively reduces the influence from the interface states by keeping the electron flow far away from the interface. It is also worth pointing out that the μ_{FE} decreases at high electric field, indicating that the conduction channel could be drawn closer to the interface resulting in the stronger influence from the interface states. Threshold voltage (V_{th}) is extracted from the intercept on the V_{gs} axis of fig. 3a by linear-fitting the data points with the greatest slope in the transfer characteristics. V_{th} at room temperature is so determined to be -0.3 V, showing slightly normally-on operation of the device. It is expected that a positive V_{th} may be achieved by further reducing the epitaxial buried-channel thickness. Fig. 3b shows I_{ds} - V_{gs} characteristics of

the same device measured at 200°C with the drain voltage fixed at 50 mV. The calculated μ_{FE} at 200°C as a function of V_{gs} in fig. 3b exhibits a substantially higher peak value of 269 cm²/Vs at low electrical field, compared to that at room temperature. The increase of the channel mobility with increasing temperature, which was also reported in [3], can be attributed to thermally activated transport of electrons. Specifically, at elevated temperature of 200°C, the electrons usually confined in the interface traps near conduction band edge may gain the extra activation energy for detrapping. In addition, the reduced numbers of filled traps especially also produce fewer Coulomb scattering centers. V_{th} at 200°C is extracted to be -1.05 V from the I_{ds} - V_{gs} curve in Fig. 2b, a slight shift towards negative direction. This shift could be understood by considering that the thermal activation at elevated temperature increases the channel electron concentration, giving rise to a smaller threshold voltage.

Conclusion: The new 4H-SiC trench gate MOSFET structure with epitaxial buried channel has been demonstrated. The fabricated devices, after undergoing the rapid thermal annealing at 850°C for Ohmic contacts, still exhibit high channel mobilities at both room temperature and 200°C. These results are significant for the fabrication of 4H-SiC power MOSFETs that requires Ohmic contacts annealing. In fact, based on the investigation of channel mobility presented in the letter, we have designed and fabricated a new structure of power 4H-SiC MOSFETs with low on-resistance, which will be reported in the near future.

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Figure captions:

Fig. 1 Cross-sectional view of a 4H-SiC trench gate MOSFET. The channel length and width of the MOSFET are 15 μm and 350 μm , respectively. The final thickness of epitaxial buried channel is 0.15 μm .

Fig. 2 Output characteristics of a 4H-SiC trench gate MOSFET (Forward I_{ds} versus V_{ds} at different V_{gs}) (a) at room temperature; (b) at 200°C

Fig. 3 Transfer characteristics (I_{ds} versus V_{gs}) of a 4H-SiC trench gate MOSFET at a fixed drain voltage of 50 mV, and field-effect mobility as a function of gate voltage (a) at room temperature; (b) at 200°C

Figure 1

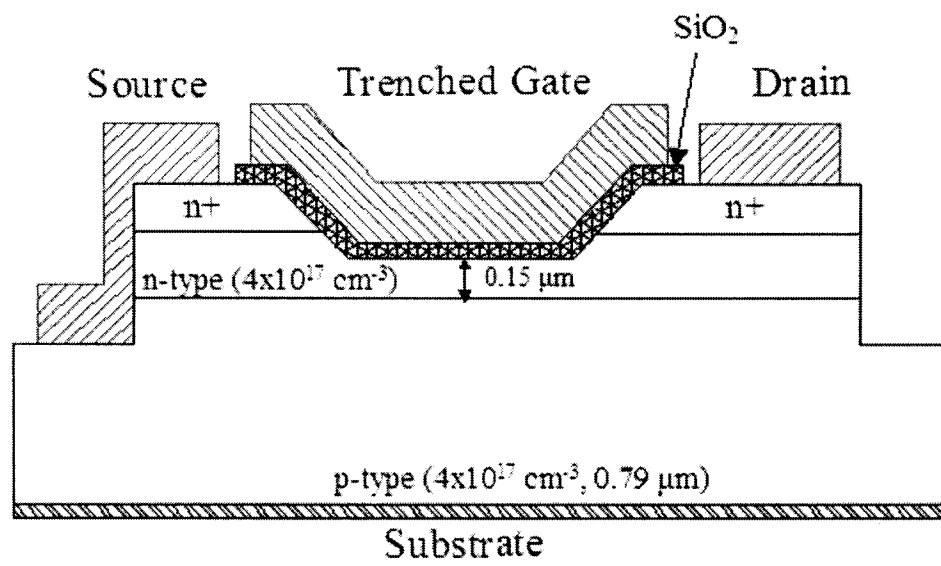


Figure 2

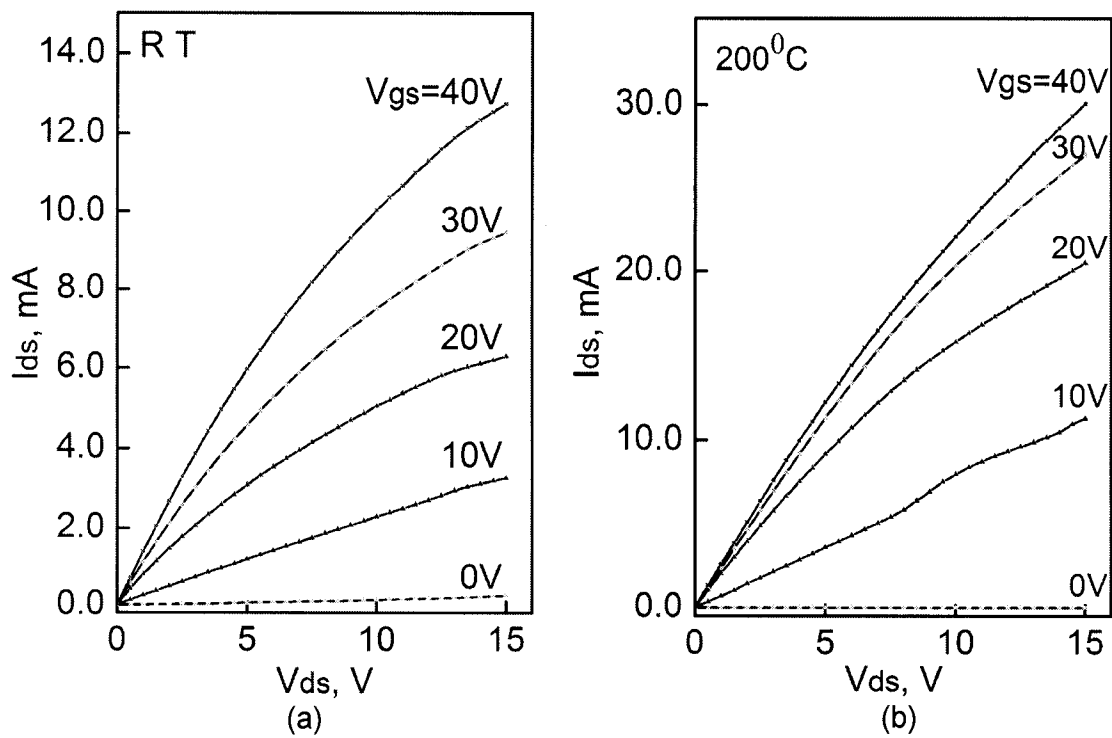


Figure 3

